

SPECIFICATION

TITLE OF THE INVENTION

INTERFACE APPARATUS

BACKGROUND OF THE INVENTION

5           This invention relates to an interface apparatus  
having a circuit emulation function. More particularly,  
the invention relates to an interface apparatus, which  
is provided between a digital transmission network, such  
as an STS-N (where N represents an integer) digital  
10 transmission network, and an ATM network, for  
eliminating an unnecessary part of frame data (e.g.,  
STS-3 data) in the digital transmission network, forming  
only the necessary part of the data into cells, sending  
the cells to the ATM network, assembling frame data  
15 (e.g., STS-3 data) of the digital transmission network  
from cells received from the ATM network, and sending  
the assembled frame data to the digital transmission  
network.

As shown in Fig. 30, a dedicated service network  
20 constituted by an optical transmission line of a SONET  
(Synchronous Optical Network) enables communication by  
connecting terminals CPE such as DS3, STS-3 or STS-12  
terminals by optical transmission lines via  
multiplexer/demultiplexers MDX and digital cross-connect  
25 systems DCCS. Dedicated service networks differ from  
ordinary telephone communication networks or the like in  
that they do not require call-connect and call-  
disconnect processing and in that entrances to and

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exists from such networks are decided in a semi-permanent manner. A DCCS has functions such as path switching, multiplexing/demultiplexing and frame add/drop but does not have a function for dynamic routing as does an exchange. For this reason, conventional dedicated service networks have problems relating to network maintenance. For example, it is not easy to carry out network rerouting and expansion (1) when it is desired to establish an alternative path between terminals owing to a decline in the quality of or the occurrence of a failure in a specific transmission path and (2) when it is desired to expand a network owing to an increase in traffic over a specific path.

Accordingly, there is demand for a dedicated service network in which network rerouting and expansion can be performed by substituting an ATM switch for a DCCS and issuing commands and making settings directly from a center. Fig. 31 is a conceptual view for a case where an OC3 DCCS is replaced by an ATM switch. In order to replace the OC3 DCCS by the ATM switch, not only are a switch ATM-SW and a controller CNTL necessary but it is also required that the transmission paths have interfaces (STS-3 CES) INF1 to INF4 through which the optical transmission lines of an OC3 SONET interwork with the ATM switch. Each of the interfaces INF1 to INF4 has a circuit emulation (CE) function. The interfaces INF1, INF2 convert STS-3 frame data, which

has been received from an optical transmission line, to ATM cells, and the interfaces INF3, INF4 assemble ATM cells into an STS-3 frame format and send the frames to an optical transmission line.

5           In a case where STS-N (where N represents an integer) frame data is converted to ATM cells in such an interface, it is necessary to convert the frame data and send it to an ATM network in such a manner that the transmission band is reduced. Moreover, it is necessary  
10       for data in the original STS-N frame format to be assembled from received cells and transmitted to a digital transmission line.

          An interface for receiving cells from an ATM network, assembling the cells into a frame format and  
15       transmitting the results to an optical transmission line is provided with a receive buffer of a prescribed capacity for two purposes, namely (1) for clock transfer and (2) to accommodate fluctuations in cell arrival. An initial fill level (IFL) is set for the receive buffer  
20       in such a manner that (1) the receive buffer will not be emptied if the ATM cell arrival interval is such that cells do not arrive over an assumed period of time and (2) the receive buffer will not overflow if the ATM cell arrival interval is such that too many cells arrive over  
25       an assumed period of time. If the IFL fluctuates so as to cause starvation or overflow of the receive buffer, the continuity of information cannot be maintained and cell discard occurs. Accordingly, it is necessary to

exercise control in such a manner that the IFL will not fluctuate even if cell loss, insertion of erroneous cells or garbling of cells, etc., occur, thereby assuring that the receive buffer will not experience starvation or overflow.

#### SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to arrange it so that STS-N frame data can be converted to ATM cells so as to reduce the transmission band, and so that the STS-N frame format can be assembled from received cells.

Another object of the present invention is to arrange it so that a large quantity of reproduced data will not be lost if P-format cells are lost, and so that an IFL that has been set for a receive buffer will not fluctuate owing to cell loss, insertion of erroneous cells or garbling of cells, etc., thereby assuring that the receive buffer will not experience starvation or overflow.

According to the present invention, (1) the part of a frame that contains a payload and overhead data, which indicates the starting position of a low-bit-rate data block multiplexed into a frame, is defined as a cell conversion zone; (2) the data in the cell conversion zone is converted cells when a prescribed position in the cell conversion zone is adopted as a reference position; and (3) a pointer that specifies the reference position is included in a prescribed cell. If this

arrangement is adopted, only the portion of the overhead that will be necessary later need be converted cells.

As a result, the amount of transmitted data can be reduced, thereby making it possible to reduce the

- 5 transmission band. Since the pointer that specifies the prescribed position (e.g., the starting position) of the cell conversion zone in a frame is incorporated in a cell, the interface on the receiving side can assemble a frame from received cells upon referring to the pointer.
- 10 A cell that contains a pointer shall be referred to as a P-format cell and a cell that does not contain a pointer shall be referred to as a non-P-format cell.

- Further, according to the present invention, a cell payload of AAL Type 1 received from an ATM network is
- 15 stored in a receive buffer in sync with the clock of the ATM network, and the cell payload is read out of the receive buffer in sync with a clock on the side of a digital transmission line, thereby performing clock transfer. Further, a pointer is detected from a cell
- 20 payload that has been read out of the receive buffer, the starting position of a cell conversion zone is identified based upon the pointer, and a frame is assembled using data output from the receive buffer based upon the starting position of the cell conversion
- 25 zone. If this arrangement is adopted, the interface can recognize the cell conversion zone in a frame and the starting position of each byte in the frame based upon the pointer, as a result of which it is possible to

assemble the original frame from the data read out of the receive buffer. In case of AAL Type 1, one cycle is constructed by eight cells and a sequence count SC (= 0 to 7) is assigned to each cell.

5 Further, according to the present invention, timing at which a succeeding pointer will appear is predicted by pointer detection. If a P-format cell does not appear at the predicted timing and the cell at this timing is an invalid cell or dummy cell, the cell is  
10 judged to be a P-format cell. Further, if an arriving cell is a cell whose sequence count SC is 6, this cell is an invalid cell or dummy cell and, moreover, a P-format cell has not yet been detected between SC = 0 and SC = 7, then the arriving cell is judged to be a P-  
15 format cell.

If this arrangement is adopted, a P-format cell can be generated even if a P-format cell is lost owing to cell loss or cell garbling, and it can be so arranged that the IFL that has been set for a receive buffer will  
20 not fluctuate. This makes it possible to assure that starvation and overflow will not occur.

Further, timing at which a succeeding pointer will appear is predicted by pointer detection. When a P-format cell is lost at the predicted timing, a  
25 prescribed cell is judged to be a P-format cell based upon this timing. This makes it possible to raise the precision with which P-format cells are judged. By virtue of the foregoing, a cell can be assumed to be a

P-format cell correctly every cycle ( $SC = 0 \sim 7$ ) and the IFL of a receive buffer can be prevented from fluctuating as a result of judging a P-format cell to be a non-P-format cell or judging a non-P-format cell to be a P-format cell. Moreover, even if a P-format cell is lost, the fact that a prescribed cell is assumed to be a P-format cell assures that a large quantity of reproduced data will not be lost as a consequence of loss of P-format cells.

Further, according to the present invention, a cell (dummy cell or invalid cell) that has a high likelihood of being a P-format cell is assumed to be a P-format cell when a P-format cell has been lost. As a result, a cell can be assumed to be a P-format cell correctly every cycle ( $SC = 0 \sim 7$ ) and therefore the IFL of a receive buffer can be prevented from fluctuating. Moreover, even if a P-format cell is lost, the fact that a prescribed cell is assumed to be a P-format cell assures that a large quantity of reproduced data will not be lost as a consequence of loss of P-format cells.

Further, according to the present invention, whether a cell having an even-numbered SC value is a P-format cell is checked successively every cycle and, when a P-format cell is lost, a cell for which SC is equal to 6 is assumed to be a P-format cell. If this expedient is adopted, a cell can be assumed to be a P-format cell through a simple arrangement and it possible to assure agreement between the bands of STS-3 and ATM

networks.

Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying  
5 drawings, in which like reference characters designate the same or similar parts throughout the figures thereof.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram useful in describing an STS-3  
10 frame format;

Fig. 2 is a diagram useful in describing cell conversion zones of an STS-3 frame;

Fig. 3 is a diagram useful in describing frame decomposition/assembly;

15 Fig. 4 is a diagram useful in describing the structure of an AAL Type 1 cell;

Fig. 5 is a diagram useful in describing the structure of an SAR-PDU header;

20 Fig. 6 is a diagram useful in describing the structure of an RTS information format;

Figs. 7A, 7B are diagrams useful in methods of identifying the boundaries of structured data;

Fig. 8 is diagram showing the overall construction of an interface on the entrance side of an ATM network;

25 Fig. 9 is a diagram illustrating a unit for creating various signals;

Fig. 10 is a diagram showing the timings of various signals;



Fig. 11 is a diagram showing the relationship between the value of a count in an STS counter and an STS-3 frame;

Fig. 12 is a diagram showing the relationship  
5 between the value of a count in an STS downcounter and an STS-3 frame;

Fig. 13 is a diagram useful in describing the generation of an STD pointer;

Fig. 14 is a diagram illustrating a unit for  
10 creating an SAR-PDU header;

Fig. 15 is a diagram illustrating a transmit-buffer write controller;

Fig. 16 is a diagram showing the structure of a transmit buffer;

15 Figs. 17A, 17B are diagrams useful in describing the mapping of SAR-PDU to a transmit buffer;

Fig. 18 is a diagram illustrating a transmit-buffer read-out controller;

Fig. 19 is a diagram illustrating the structure of  
20 an ATM cell creating unit;

Fig. 20 is diagram showing the overall construction of an interface on the exit side of an ATM network;

Figs. 21A, 21B are diagrams useful in describing writing to a receive buffer and read-out from the  
25 receive buffer;

Fig. 22 is a diagram showing the construction of an interface provided on the exit side of an ATM network and having a band adjustment function;

Fig. 23 is a diagram useful in describing the output of a selector;

Fig. 24 is a flowchart illustrating processing for detecting pointers and judging P-format cells;

5        Fig. 25 is a diagram showing another construction of an interface on the exit side of an ATM network having a band adjustment function;

Fig. 26 is a flowchart illustrating pointer correction processing;

10       Fig. 27 is a diagram showing a third embodiment of an interface on the exit side of an ATM network having a band adjustment function;

Fig. 28 is a flowchart illustrating pointer correction processing;

15       Fig. 29 is a diagram showing a fourth embodiment of an interface on the exit side of an ATM network having a band adjustment function;

Fig. 30 is a diagram illustrating a dedicated service network constituted by SONET transmission lines;

20       and

Fig. 31 is a diagram illustrating an ATM having a CE function.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

(A) Overview of the invention

25       (a) Frame format

Though the present invention is applicable generally to STS-N (where N represents an integer) frames, a case in which the invention is applied to an

STS-3 frame will be described below.

Fig. 1 is a diagram useful in describing an STS-3 frame format. A 155.52-Mbps STS-e frame is obtained by multiplexing three 50-Mbps frames and adding on  
5 overhead. The STS-3 frame is composed of  $9 \times 270$  bytes. The initial  $9 \times 9$  bytes constitutes overhead OH and the remaining  $9 \times 261$  bytes constitutes a payload SPE. The overhead OH is composed of section overhead SH, line  
10 overhead LH and a 9-byte pointer PT. Section overhead SH is for transmitting a frame synchronizing signal and a repeater-section error monitoring signal, and line overhead LH is for transmitting a multiplex-section error monitoring signal and a multiplex-section status signal (AIS/FERF: Alarm Indication Signal / Far-End  
15 Receive Failure). The pointer PT indicates the starting positions of the three multiplexed STS-1 frames and is used when decomposing the STS-3 frame into the STS-1 frames.

(b) Cell conversion zone

20 When such STS-3 frame data is converted to ATM cells and transmitted, it is necessary to reduce the transmission band and construct the original STS-3 frame data from received cells on the receiving side. The part of the data to be transmitted is reduced in order  
25 to reduce the transmission band. Accordingly, the structure of the STS-3 frame is taken into consideration, the portion unnecessary for the network of the other party is deleted and only the portion truly

required undergoes cell conversion, thereby reducing the quantity of information. Fig. 2 is a diagram useful in describing the cell conversion zone of an STS-3 frame.

There are four types of cell conversion zones, which are  
5 as follows:

(1) With a first cell conversion zone (No. 1), only the payload SPE is transmitted. In accordance with the first cell conversion zone, the transmission band can be reduced. In order to achieve transmission  
10 without omission, however, it is necessary to terminate the path layer, decompose the STS-3 frame into three STS-1 frames and transmit the frames on three connections. If the STS-1 SPE level has a steady deviation, it is required that asynchronous clocking be  
15 carried out.

(2) With a second cell conversion zone (No. 2), the pointer PT and payload SPE are transmitted. In accordance with the second cell conversion zone, transmission can be achieved by a single connection. In  
20 addition, transmission based upon synchronous clocking can be performed and, moreover, the transmission band can be made comparatively small.

(3) With a third cell conversion zone (No. 3), the pointer PT, line overhead LH and payload SPE are  
25 transmitted. In accordance with the third cell conversion zone, transmission can be achieved by a single connection. In addition, though transmission based upon synchronous clocking can be performed, the

fact that the line overhead LH is transmitted means that the transmission band is broadened in comparison with the second cell conversion zone.

(4) With a fourth cell conversion zone (No. 4),  
5 all frame data (pointer PT, section overhead SH, line overhead LH and payload SPE) is transmitted. In accordance with the third cell conversion zone, transmission can be achieved by a single connection. In addition, though transmission based upon synchronous  
10 clocking can be performed, the fact that section overhead SH and line overhead LH are transmitted means that the transmission band is broadened in comparison with the second cell conversion zone.

When the four cell conversion zones described above  
15 are considered, it will be appreciated that the second cell conversion zone is best. According to the present invention, therefore, the hatched portion (pointer PT and payload SPE) indicated by the second cell conversion zone is converted to cells and transmitted, as shown in  
20 Fig. 3, to reduce the amount of transmitted information. Since termination of the section layer and line layer has been requested by the user, no problems arise even when section overhead SH and line overhead LH are deleted.

25 (c) Method of identifying structured data

When STS-3 frame data is converted to cells and transmitted, as shown in Fig. 3, the interface at the exit of the ATM network must be capable of assembling

the original STS-3 frame data from the received cells.  
To achieve this, an arrangement must be adopted in which  
it is possible to recognize a reference position in the  
cell conversion zone of the STS-3 frame, e.g., the  
5 initial byte position (row 1, column 10) TOP of the  
payload SPE. Hence, according to the present invention,  
AAL Type 1 (ATM Adaptation Layer Type 1) cells are used  
as the ATM cells and the reference position TOP of the  
cell conversion zone is designated by an SDT pointer  
10 (Structured Data Transfer pointer) of an AAL Type 1  
Cell. If this arrangement is adopted, the interface on  
the cell receiving side recognizes an SDT-pointer-  
containing cell by a CSI (Convergence Sublayer  
Identifier) included in the SAR-PDU header of an AAL  
15 Type 1 cell, recognizes the reference position TOP based  
upon the SDT pointer of this cell and can assemble the  
original STS-3 frame data. It should be noted that the  
section overhead SH and line overhead LH are created  
independently and inserted into the STS-3 frame format.  
20 Fig. 4 is a diagram useful in describing the format  
of an AAL Type 1 (AAL-1) ATM cell, and Fig. 5 is a  
diagram useful in describing the format of a 1-byte SAR-  
PDU. The first five bytes of an AAL-1 cell constitute  
the ATM header and the remaining 48 bytes constitute the  
25 cell payload (information field). The information field  
is composed of a 1-byte SAR-PDU (PSU stands for  
"Protocol Data Unit") header and a 47-byte SAR-PDU  
payload. The SAR-PDU payload is used to transfer user

data, and the SAR-PDU header is composed of a 4-bit SN (Sequence Number) field and a 4-bit SNP (Sequence Number Protection) field, as illustrated in Fig. 5.

The SN field is divided into two subfields, namely a CSI (Convergence Sublayer Identifier) and SC (Sequence Count), and the SNP field also is divided into two subfields, namely a CRC (Cyclic Redundancy Check) and EPB (Even Parity Bit). The SC subfield counts cells cyclically from 0 to 7 (i.e., 0, 1, ..., 7, 0, 1, ..., 7, 0, 1, ...) and makes it possible to monitor the sequence of the cells and to detect cell loss and erroneous cell insertion. Error detection and correction of the SN field are performed by the CRC and EPB subfields.

The CRC is a value based upon a polynomial  $[G(X) = X^3 + X + 1]$  with respect to the sequence number. The EPB is an even-numbered parity bit in the SAR-PDU header. The CSI bit is the CS (Convergence Sublayer) function of the AAL-1 cell and is used to send and reproduce the timing information of the user clock and to transfer the SDT pointer.

Transmission and reproduction of user-clock timing information is by the SRTS (Synchronous Residual Time Stamp) method. In accordance with the SRTS method, the timing information of the user clock is composed of 4-bit information (RTS4, RTS3, RTS2, RTS1) referred to as an RTS (Residual Time Stamp). This RTS information is transferred by the CSI bit every eight cells, as

depicted in Fig. 6. That is, a multiframe (one cycle) is constituted by eight AAL-1 cells ( $SC = 0 \sim 7$ ). The CSI has an 8-bit structure ( $CSI_0$  to  $CSI_7$ ) corresponding to SC values of 0 to 7, respectively. Four-bit RTS information RTS1 ~ RTS4 is sent by CSI bits ( $CSI_1$ ,  $CSI_3$ ,  $CSI_5$ ,  $CSI_7$ ) of ATM cells whose SC values are 1, 3, 4, 7. This 4-bit RST information RTS1 ~ RTS4 is the count of a 4-bit counter obtained when a network clock is cyclically counted by a 4-bit counter and a clock on the transmitting side is frequency divided by 3008 and pulses resulting from this frequency division are generated. By transmitting this RTS information, a clock synchronized to the clock on the transmitting side can be generated on the cell receiving side and data can be transmitted to a terminal in sync with this clock. It should be noted that the figure of 3008 mentioned above is the number (8 cells  $\times$  47 bytes  $\times$  8 bits) of bits of user data in eight ATM cells.

When  $n \times 64$ -kbps-structured data (where  $n = 9 \times 270 = 2430$  in case of STS-3) is transferred, the SDT pointer describes the boundary (e.g., the beginning of the frame) of the structured data. As shown in Figs. 7A and 7B, there are two format types (P-format, which means existence of a pointer, and non-P-format, which means absence of a pointer) depending upon the CSI indication ("1", "0") of a cell having an even-numbered SC value (i.e., a cell whose SC value is 0, 2, 4 or 6). If the format is the P-format, for which  $CSI = "1"$  holds, the



value of the initial byte position (pointer field) of the SAR-PDU payload of the cell is the SDI pointer, and the remaining 46 bytes constitute the user information (Fig. 7A). The content set in the pointer is the

5 offset, expressed in byte units using binary notation, from the end of the pointer field to the boundary (frame starting position) of the structured data. The payload ranges from the remaining 46 bytes of the SAR-PDU payload of this cell to the 47 bytes of the SAR-PDU of

10 the next cell (i.e., a cell having an odd-numbered SN). Values of 0 to 93 can be set. Fig. 7A illustrates a case where the boundary of the structured data resides in a cell having an even-numbered SC value, and Fig. 7B illustrates a case where the boundary of the structured

15 data resides in a cell having an odd-numbered SC value.

Thus, in accordance with the present invention, (1) when STS-3 frame data is converted to ATM cells and transmitted, the AAL-1 cell conversion zone is made the hatched portion in Fig. 3, as a result of which the

20 transmission band can be reduced, and (2) the reference position of the cell conversion zone is specified using the SDT pointer of the AAL-1 cell, as a result of which the original STS-3 frame data can be reconstructed from received cells by the interface on the exit side of the

25 ATM network. Section overhead and line overhead are generated independently. More specifically, in accordance with the present invention, an SDT pointer is used and the starting position of reduced data is placed

in an ATM cell as information, thereby making it possible to reduce the required band (amount of information) while maintaining the STS-N format of the existing network.

- 5           (d)   Necessity of control for fixing level of  
                  receive buffer

The interface on the ATM-cell receiving side is internally provided with a receive buffer for storing received user information. The receive buffer is a  
10   play-out buffer provided for two purposes, namely (1) for clock transfer and (2) to accommodate fluctuations in cell arrival. Though a play-out buffer basically is a FIFO buffer, it possesses an initial fill level (IFL) and data cannot be read out of the buffer until data  
15   accumulates in the buffer up to the IFL. Through use of a receive buffer, generally a clock transfer is made from the data highway clock in an ATM switch to the clock of a line. The reason for this is that an ATM network usually operates with a common clock having a  
20   speed higher than line speed and cannot send data out to the line as is.

When an ATM cell is transferred within an ATM network, on the other hand, the arrival interval on the receiving side usually is not uniform even if ATM cells  
25   are transmitted at regular intervals. The reason for this is that the switching of ATM cells is not based upon fixed slot multiplexing such as in line switching but is instead based upon statistical multiplexing.

That is, with statistical multiplexing, a transfer band for each line exists as far as probability is concerned and therefore a delay added on by the ATM switch takes on a value that differs cell by cell. A variation in  
5 amount of delay added onto cells is referred to as CDV (Cell Delay Variation). A tolerance value is decided in dependence upon the service type and class type, etc., of the ATM connection, and quality control is carried out in such a manner that the CDV value will fall within  
10 this tolerance value. When the interval at which cells arrive at the receive buffer is observed, therefore, the interval will vary within a fixed range. However, if observation is carried out over a comparatively long period of time, the frequency with which cells arrive  
15 will be a value decided by the line rate.

The initial fill level (IFL) of the receive buffer is set to a value that will enable the assumed (allowed) CDV to be accommodated. Specifically, the IFL is made a value such that:

20       ·the receive buffer will not be emptied if the ATM cell arrival interval is such that cells do not arrive over an assumed period of time; and

      ·the receive buffer will not overflow if the ATM cell arrival interval is such that too many cells arrive  
25 over an assumed period of time. In other words, it should be possible to tolerate a widening of the cell arrival interval with leeway from empty up to the IFL and to tolerate a narrowing of the cell arrival interval

with leeway from the IFL to the maximum buffer capacity.

Though the quantity of cells which reside in a receive buffer usually fluctuates with the IFL serving as the center value, the average center value over a comparatively long period of time becomes the IFL. If the IFL is made sufficiently large in comparison with the assumed CDV and the buffer depth also is made sufficiently large, a correspondingly large leeway will be obtained and it will be possible to tolerate a CDV beyond what is expected. However, making the receive buffer larger than necessary lengthens the time necessary for cells to pass through the buffer and enlarges the CTD (Cell Transfer Delay) of the network transmission. Accordingly, the IFL and buffer depth are set to values just large enough to accommodate the assumed CDV.

Consider a situation where noise is picked up in the process of transferring a cell and that a P-format cell is mistaken for a non-P-format cell. The center value of the receive buffer in such case will become a value that is one octet larger than the IFL. The reason for this is that whereas the user data area possessed by a P-format cell is 46 octets, the user data area in the case of a non-P-format cell is 47 octets. Conversely, if a non-P-format cell is mistaken for a P-format cell for some reason, the center value of the receive buffer will become a value that is one octet smaller than the IFL. The problem in this case where a P-format cell

(non-P-format cell) is interpreted as being a non-P-format cell (P-format cell) is that an event which will offset the shift in the level of the receive buffer and restore the level to what it was originally does not  
5 take place. This means that the shift accumulates whenever it occurs. If the  $P \rightarrow \text{non-P}$ ,  $\text{non-P} \rightarrow P$  garbling occurs in alternating fashion, the above-mentioned problem will not arise but one cannot rely upon the chance that this will be the case. The problem  
10 will eventually manifest itself as a shift in the center value, i.e., as a decline in the ability to tolerate the CDV. Even though the value is within the assumed range of CDV values, starvation or overflow will occur.

Thus, it is necessary to exercise control in such a  
15 manner that the initial fill level (IFL) of the receive buffer will not fluctuate even if cell loss, erroneous cell insertion and cell garbling occur, and to so arrange it that the receive buffer will not experience starvation or overflow. According to the present  
20 invention, (1) an assumption is made that a P-format cell (an even-numbered cell for which the SC value is "1") always exists in one cycle (see the multiframe of Fig. 6) of SC values of 0 to 7, and (2) if a boundary of structured data does not exist in one cycle, a cell for  
25 which the SC value is 6 is forcibly adopted as a P-format cell and the SDT pointer value is made 127. (2) Furthermore, according to the present invention, an SN continuity and CRC check / parity check is performed

and an indication as to whether a cell is valid/invalid  
or a dummy cell is added to the SNP field. As a result,  
if a P-format cell does not exist in one cycle, it can  
be assumed that a cell onto which the invalid-cell  
5 indication has been added or a cell onto which the  
dummy-cell indication has been added is a P-format cell.  
If two P-format cells exist in one cycle, it can be  
assumed that a cell having the valid-cell indication is  
a P-format cell. If a correct P-format cell can thus be  
10 assumed to be present in one cycle, then a P-format cell  
will no longer be judged to be a non-P-format cell and a  
non-P-format cell will no longer be judged to be a P-  
format cell. This makes it possible to prevent the IFL  
of a receive buffer from fluctuating and to prevent the  
15 loss of a large quantity of reproduced data.

(B) Interface on entrance-side of ATM network

(a) Overall construction

Fig. 8 is a diagram showing the overall  
construction of an interface on the entrance side of an  
20 ATM network. An STS-3 line termination unit 10 receives  
STS-3 frame data from an OC3 transmission line, outputs  
a signal SPETOP at the timing of the reference position  
TOP (the position of the byte at row 1, column 10) of  
the cell conversion zone in the frame, and outputs the  
25 pointer POT and payload SPE of the AAL-1 cell conversion  
zone (the hatched portion) as frame data UPDAT. An AAL-  
1 cell generating unit 20 converts the entering frame  
data UPDAT into AAL-1 cells, incorporates the SDT

pointer, which indicates the reference position TOP,  
into a prescribed AAL-1 cell and sends the cell to an  
ATM network.

The AAL-1 cell generating unit 20 includes a signal  
5 creation unit (SSRTS) 21 for creating various signals  
such as an SDT pointer (PTR), a transmit signal RTS, an  
SC count value (SC) and a pointer-creation indication  
signal (PTREN); an SAR-PDU creation unit (SAAL1) 22 for  
creating an SAR-PDU header (PDUHDR) using the RTS  
10 information, SC count value and pointer-creation  
indication signal, etc.; a transmit-buffer write  
controller (SRWC) 23 for suitably selecting the SAR-PDU  
header (PDUHDR), SDT pointer (PTR) or frame data (UPDAT)  
and outputting the same as transmit-buffer write data  
15 (cell payload) SBWDAT; a transmit buffer (SBUF) 24,  
which comprises a FIFO buffer, for storing the 48-byte  
cell payload input thereto and successively outputting  
the same in response to a read-out request; a transmit-  
buffer read-out controller (SBRC) 25 for successively  
20 reading out and outputting the cell payload from the  
transmit buffer 24 in response to a request from an ATM  
cell creation unit; and an ATM cell creation unit (ATM)  
26 for adding a 5-byte ATM header onto the cell payload,  
thereby creating an ATM cell, and sending the ATM cell  
25 to the ATM network.

(b) Signal creation unit 21

Fig. 9 is a diagram illustrating the construction  
of the signal generation unit 21 and Fig. 10 is a timing

chart of the various signals. The reference-position  
signal SPETOP from the STS-3 line termination unit 10  
and a master clock (byte timing pulse) UPCLK of the line  
on the upstream side enter the signal generation unit  
5 21, and so does a 155.52-Mbps network clock, which is  
for RTS operation, that arrives from the ATM network.

An STS counter 21a is a counter that indicates each  
of 2430 ( $= 9 \times 270$ ) byte positions in an STS-3 frame  
(see Fig. 11). (1) The STS counter 21a is preset to a  
10 numerical value of 9 by the reference-position signal  
SPETOP, (2) counts the byte timing pulses UPCLK and (3)  
outputs an STS-3 overhead indication signal RXOH, which  
takes on the logical "1" value at the byte positions of  
the section overhead SH and line overhead LH.

15 A payload-octet position creation unit 21b outputs  
the octet positions (0 ~ 46) of the SAR-PDU payload.  
More specifically, the payload-octet position creation  
unit 21b counts the byte timing pulses UPCLK (Fig. 10)  
in the AAL-1 cell conversion zone indicated by the bold  
20 border in Fig. 12 (namely when the STS-3 overhead  
indication signal RXOH is logical "0") and outputs the  
octet position (0 ~ 46) of the SAR-PDU payload as a  
signal OCTET. The payload-octet position creation unit  
21b further outputs an SC enable signal (SCEN) whenever  
25 the numerical value OCTET becomes zero. A sequence  
count creation unit 21c counts the SC enable signal SCEN  
and outputs the sequence count (SC) of 0 ~ 7. An RTS  
latch timing creation unit 21d outputs a latch pulse LT



at OCTET = 0 and SC = 0, a 4-bit RTS counter 21e counts the network clock cyclically, and a counter-value latch circuit 21f latches and outputs, as the transmit RTS information RTS1 ~ RTS4, the content (four bits) of the  
5 RTS counter 21e prevailing when the latch pulse LT is generated.

An SDT pointer creation unit 21g has a downcounter DCNT for indicating each of 2358 byte positions in the AAL-1 cell conversion zone (the area enclosed by the  
10 border in Fig. 12) of the STS-3 frame. The downcounter DCNT (1) is preset to the numerical value 2357 by the reference-position signal SPETOP and (2) is decremented whenever the byte timing pulse UPCLK is generated in the AAL-1 cell conversion zone (namely when the STS-3  
15 overhead indication signal RXOH is logical "0"), thereby outputting 2357 ~ 0 repetitively. If the numerical value is 93 ~ 1 when the sequence count value SC is an even number and payload octet position signal OCTET = 0 holds, then the SDT pointer creation unit 21g outputs  
20 this numerical value as an SDT pointer value PTRV and outputs the pointer-creation indication signal PTREN. Fig. 13 is a diagram useful in describing SDC pointer generation. Since the value in the downcounter DCNT lies in the range 93 ~ 1 when SC = 4 (even number) and  
25 OCTET = 0 hold, the value at this time (= 89) is output as the SDT pointer value PTRV. A parity creation unit 21h creates even-numbered parity of the SDT pointer value. An 8-bit SDC pointer is constructed by the 7-bit

SDT pointer value PTRV and 1-bit parity.

As mentioned above, the SDT pointer creation unit  
21g decides an SDT pointer to indicate which cell of one  
cycle (SC = 0 ~ 7) is to serve as a P-format cell and  
5 then calculates the SDT pointer to be applied.  
Specifically, the following rule is observed to generate  
the SDT pointer:

(1) An AAL-1 cell (P-format cell) having an SDT  
pointer always appears only once in one cycle, where SC  
10 values of 0 to 7 constitute one cycle.

(2) Only an AAL-1 cell for which SC is an even  
number (0, 2, 4, 6) can be a P-format cell. Further,  
the SDT pointer can take on values of 0 to 93 and 127.

(3) When the current cycle is devoid of a  
15 structured-data boundary and the beginning of the  
payload of the cell for which SC = 0 holds in the next  
cycle also is not a structured-data boundary, the cell  
for which SC = 6 holds in the current cycle becomes the  
P-format cell and the SDT pointer value is "127" (all  
20 "1"s).

(4) When a structured-data boundary exists at the  
beginning of the payload of the cell for which SC = 0  
holds, the cell for which SC = 0 holds becomes the P-  
format cell and the SDT pointer value is "0". When a  
25 structured-data boundary does not exist in the  
immediately preceding cycle in this case, the cell for  
which SC = 6 holds in the immediately preceding cycle  
becomes the P-format cell and the SDT pointer value

becomes "93".

(5) When a structured-data boundary exists at the beginning of the payload of a cell for which SC = 2 (or 4, 6) holds, the cell for which SC = 2 (or 4, 6) holds becomes the P-format cell and the SDT pointer value becomes "93".

(c) SAR-PDU header creation unit (SAAL1) 22

Fig. 14 is a diagram illustrating the construction of the SAR-PDU header creation unit 22. A CSI creation unit 22a (1) outputs CSI = RTS information (RTS1 ~ RTS4) when the sequence count SC (0 ~ 7) is an even number; (2) outputs CSI = "1" if the SDR pointer-creation indication signal PTREN is "1" when the SC value is an odd number; (3) and outputs CSI = "0" if the SDR pointer-creation indication signal PTREN is "0" when the SC value is an odd number. A CRC creation unit 22b creates a 3-bit CRC in accordance with a predetermined CRC calculation equation using the SN field (CSI + SC), and a parity creation unit 23c creates even-numbered parity EPB for the seven bits of (CSI + SC + CRC). The SAR-PDU header creation unit 22 outputs CSI, SC, CRC and EPB as the SAR-PDU header (PDUHDR) cell by cell.

(d) Transmit-buffer write controller 23

Fig. 15 is a diagram showing the construction of the transmit-buffer write controller 23. A selector 23a suitably selects the SAR-PDU header (PDUHDR), SDT pointer PTR or STS-3 frame data UPDAT based upon the payload octet position signal OCTET and pointer-creation

indication signal PTREN. As a result, the selector 23a sends transmit-buffer write data (cell payload) to the transmit buffer 24. A transmit-buffer write address creation unit 23b controls the generation of an address (SBWADR) for writing a cell payload to the transmit buffer and the generation of a write-enable signal (SBWEN). More specifically, (1) when transmit buffer full SBFULL = "1" holds at the payload octet position OCTET = 0 (start timing of the SAR-PDU), the transmit-buffer write address creation unit 23b regards this as transmit-buffer overflow and does not write data to the transmit buffer. (2) When transmit buffer full SBFULL = "0" holds at the payload octet position OCTET = 0, the transmit-buffer write address creation unit 23b generates the write-enable signal (SBWEN) and writes data to the transmit buffer. (3) The transmit-buffer write address creation unit 23b halts the write operation in a period of time corresponding to an AAL-1 cell conversion byte indicated by the STS-3 overhead indication signal RXOH = "1". (4) When writing of data has started, the transmit-buffer write address creation unit 23b outputs a write-completion signal SBWCOMP at the timing of OCTET = 46.

(e) Transmit buffer

Fig. 16 is a diagram showing the construction of the transmit buffer 24, which is constituted by an FIFO buffer and is capable of storing a maximum of four cells. A cell payload in the non-P-format is mapped to

the transmit buffer in the manner shown in Fig. 17A, and cell payload data in the P-format is mapped to the transmit buffer in the manner shown in Fig. 17B.

(f) Transmit-buffer read-out controller 25

5        Fig. 18 is a diagram illustrating the construction of the transmit-buffer read-out controller 25. An ATM cell timing creation unit (53-octet counter) 25a drives the 53-octet counter by the highway clock within the switch and creates a 53-octet signal HTP that indicates  
10    the beginning of the ATM cell. A transmit-buffer read-out address creation unit 25b (1) generates a read-out address SBRADR for the transmit buffer 24 based upon the ATM cell timing, and (2) creates the transmit buffer full signal SBFULL and a transmit-buffer non-empty  
15    signal (reverse logic of transmit-buffer empty) \*SBEMPTY based upon the write-completion signal SBWCOMP from the transmit-buffer write controller 23 and a read-out request SBRC from the ATM cell creation unit 26.

      The transmit buffer 24 is a FIFO buffer for a  
20    maximum of four cells, as mentioned above. The transmit-buffer read-out controller 25 monitors the amount of use of this buffer to thereby detect transmit-buffer overflow, inhibit the writing of data anew (i.e., discard data that the apparatus is attempting to write  
25    in) and notify of the occurrence of overflow. A pointer is used to manage the amount of buffer used. A write pointer (SBW\_PTR) and a read-out pointer (SBR\_PTR) are provided internally as the pointers. Both pointers can

take on values of 0 to 3. The particular value indicates the logical address (in cell-payload units) of the transmit buffer.

The trigger that advances the write pointer SBW\_PTR is entry of the write-completion signal SBWCOMP from the transmit-buffer write controller 23. The trigger that advances the read-out pointer SBR\_PTR is entry of the read-out request SBRC from the ATM cell creation unit 26; this is the time at which read-out processing is completed. Furthermore, there are two buffer states, namely transmit-buffer empty SBEMPTY and transmit-buffer full SBFULL, which indicate that the transfer buffer is empty and full, respectively, when their logic values are "1". The ATM cell creation unit 26 issues the read-out request command SBRC if the transmit buffer is not empty (\*SBEMPTY = "1") at the timing at which the output of the transmit buffer 24 is accepted.

By using the above-mentioned pointers, the transmit-buffer read-out address creation unit 25b manages the amount of transmit-buffer use as follows:

(1) When the read-out request SBRC is received, the address creation unit 25b starts read-out processing based upon the read-out pointer SBR\_PTR. The address creation unit 25b advances the read-out pointer SBR\_PTR at completion of read-out and resets transmit-buffer full SBFULL to 0 if SBFULL = 1 holds at this time. The address creation unit 25b compares the read-out pointer SBR\_PTR after the updating thereof and the write pointer

SBW\_PTR. If SBR\_PTR = SBW\_PTR holds, the transmit  
buffer 24 is emptied by the current read-out; the next  
read-out cannot be allowed under these conditions.  
Accordingly, \*SBEMPTY = 0 is set. As a result, the  
5 read-out request SBRC no longer arrives from the ATM  
cell creation unit 26.

(2) When the write-completion notification signal  
SBWCOMP is received, the transmit-buffer read-out  
address creation unit 25b advances the write pointer  
10 SBW\_PTR. If transmit-buffer parity SBEMPTY = 1 holds at  
this time, SBEMPTY is reset to 0. The address creation  
unit 25b compares the write pointer SBW\_PTR after the  
updating thereof and the read-out pointer SBR\_PTR. If  
SBW\_PTR = SBR\_PTR holds, this indicates that the  
15 transmit buffer 24 was filled by the current writing of  
data; writing of the next cell payload cannot be allowed  
under these conditions. Accordingly, transfer-buffer  
full SBFULL = 1 is set.

(g) ATM cell creation unit 26

20 Fig. 19 is a diagram showing the construction of  
the ATM cell creation unit 26. A read-out request  
generator 26a sends the read-out request SBRC to the  
transmit-buffer read-out controller 25 when the transmit  
buffer 24 is not empty. An ATM-header application  
25 timing creation unit 26b outputs a header selection  
signal HSL based upon the signal HTP indicating the  
beginning of the ATM cell. A selector 26c selects and  
outputs the ATM cell header if header selection signal

HSL is "1" and selects and outputs transmit-buffer read-out data (the cell payload) at all other timings.

(B) Interface on exit-side of ATM network

Fig. 20 is a diagram showing the overall  
5 construction of an interface on the exit side of an ATM network. A cell filter 50 subjects cells that enter from an ATM highway to filtering based upon VPI/VCI values and selects/passes cells that it itself is to process. A cell determination unit 51 has a cell  
10 valid/invalid judging unit 52 and a cell loss / erroneous insertion examining unit 53. The cell valid/invalid judging unit 52 checks the SN/SNP field of the SAR-PDU header of each individual cell that has passed through the cell filter 50, i.e., performs a CRC  
15 check and parity check concerning each cell and judges the normality of the SAR-PDU header information. A 1-bit error of the CRC is capable of being corrected and is corrected. The result of the cell valid/invalid judgment is "valid" or "invalid" and is reported to the  
20 cell loss / erroneous insertion examining unit 53. An "invalid" judgment means that an SAR-PDU header has been received but cannot be trusted.

In accordance with a sequence-number check algorithm (SN check algorithm), the cell loss /  
25 erroneous insertion examining unit 53 checks for loss and erroneous insertion of cells based upon the judgment made by the cell valid/invalid judging unit 52 and the continuity of the sequence count SC in the SN field and,



on the basis of the check, decides to load a received cell into a receive buffer 57 or to discard the cell or, if cell loss has been determined, to insert a dummy cell.

5           A cell accumulator 54 stores temporarily a cell which the cell loss / erroneous insertion examining unit 53 is currently examining to determine whether or not it should be introduced to the receive buffer. If the cell loss / erroneous insertion examining unit 53 has decided  
10 that cell loss has occurred, a dummy cell creation unit 55 creates and outputs the data of the dummy cell that corresponds to the lost cell. On the basis of the decision made by the cell loss / erroneous insertion examining unit 53 to load a cell, discard a cell or  
15 insert a dummy cell, a selector 56 selects and outputs a cell from the cell accumulator 54 or a dummy cell from the dummy cell creation unit 55. Further, the selector 56 divides a 48-byte cell payload into 12 bytes four times in parallel fashion and assembles these bytes as  
20 shown in Fig. 21A, whereupon the payload is input to the receive buffer 57.

The receive buffer 57 is a play-out buffer provided for two purposes, namely (1) for clock transfer and (2) to accommodate fluctuations in cell arrival. The  
25 receive buffer 57 has a capacity for storing a prescribed number of cell payloads (SAR-PDU header + 47-byte information).

A receive-buffer controller 58 outputs a write-

enable signal WREN, a write address signal WRADD, a  
read-out-enable signal DREN, a read-out address signal  
RDADD, a latch-enable signal LATCHEN, a select signal  
RDPHASE and the reference-position signal SPETOP. More  
5 specifically, the receive-buffer controller 58 holds the  
write address signal WRADD, generates the write-enable  
signal WREN whenever data is output from the selector  
56, synchronizes this data to the write clock, writes  
this data to the receive buffer 57 and increments the  
10 write address signal WRADD. As long as the receive  
buffer 57 is not empty, data is read out of the receive  
buffer continuously in sync with the read-out clock.

When write is enabled (WREN = "1"), the receive  
buffer 57 writes the SAR-PDU data 12 bytes at a time to  
15 the address designated by the write address signal  
WRADD. When read-out is enabled (RDEN = "1"), the  
receive buffer 57 reads out the SAR-PDU data 12 bytes at  
a time from the address designated by the read-out  
address signal RDADD. If latch-enable LATCHEN = "1"  
20 holds, a latch circuit 59 latches data read out of the  
receive buffer and continues outputting latched data to  
a selector 60 constantly.

A pointer detector 61 detects the SDT pointer PTR  
from the two high-order bits of the payload read out of  
25 the receive buffer 57 and inputs a pointer value and a  
pointer-detection signal PTR-DET to the receive-buffer  
controller 58. The latter is internally provided with a  
frame counter 58a that counts from 0 to 2429 for the

5 outputs the reference-position signal SPETOP at the time  
at which counted value becomes equal to 9, namely at the  
timing of the frame reference position TOP (the starting  
position of the AAL-1 cell conversion zone).

(1) if the input to the selector 60 is data of the 12 most significant bytes of a cell payload and the second byte is the SDT pointer [see (1) in Fig. 21B], then the receive-buffer controller 58 outputs the select signal RDPHASE so as to select ten bytes starting from the third byte;

(2) if the input to the selector 60 is data of the  
25 12 most significant bytes of a cell payload and the  
second byte is user data [see (2) in Fig. 21B], then the  
receive-buffer controller 58 outputs the select signal  
RDPHASE so as to select 11 bytes starting from the

second byte;

(3) if the input to the selector 60 is data other than data of the 12 most significant bytes of a cell payload [see (3) in Fig. 21B], then the receive-buffer controller 58 outputs the select signal RDPHASE so as to  
5 select 12 bytes starting from the first byte; and

(4) during the period of time over which an STS-3 frame assembler 62 generates section overhead SH and line overhead LH, the receive-buffer controller 58 sets  
10 the select signal RDPHASE to "0000" to cause dummy data "00000000" to be output from the selector 60.

Thus, the selector sends the user data indicated by the hatching in Fig. 21B to the STS-3 frame assembler 62 at the byte timing of the AAL cell conversion zone and  
15 outputs dummy data in the overhead interval.

The STS-3 frame assembler 62 assembles the user data, which enters from the selector 60 at the byte timing of the AAL cell conversion zone, into the STS-3 frame format, creates the section overhead SH and line  
20 overhead LH at the overhead byte timing, embeds the created overhead in the overhead field to complete the STS frame data and then sends this data to the STS-3 transmission line.

(C) First embodiment of interface having band  
25 adjustment function

The data that has been read out of the receive buffer 57 is subjected to a band adjustment. By assuming that a dummy cell or invalid cell, which was

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presumed to be a P-format cell, is a P-format cell, the  
band adjustment prevents loss of a large quantity of  
reproduced data due to loss of a P-format cell and  
prevents the initial fill level (IFL) of the receive  
5 buffer from fluctuating.

Fig. 22 is a diagram showing the construction of an  
interface provided on the exit side of an ATM network  
and having a band adjustment function. Components  
identical with those shown in Fig. 20 are designated by  
10 like reference characters. This arrangement differs in  
that (1) an SAR-PDU header creation unit 71 is provided;  
(2) the cell determination unit 51 outputs a cell-header  
valid/invalid determination signal INV and a dummy-cell  
data insertion signal DUM; and (3) the pointer detector  
15 61 is replaced by a pointer detector / P-format cell  
detector 72.

The cell valid/invalid judging unit 52 subjects  
each individual cell that has passed through the cell  
filter 50 to a CRC check and parity check, judges the  
20 normality of the SAR-PDU header information and outputs  
the cell-header valid/invalid determination signal INV.  
INV = "0" signifies "valid" and INV = "1" signifies  
"invalid", i.e., the fact that an SAR-PDU header has  
been received but appears to be erroneous.

25 In accordance with an SN check algorithm, the cell  
loss / erroneous insertion examining unit 53 checks for  
loss and erroneous insertion of cells based upon the  
judgment made by the cell valid/invalid judging unit 52

and the continuity of the sequence count SC in the SN field and, on the basis of the check, decides to load a received cell into the receive buffer 57 or to discard the cell or, if cell loss has been determined, to insert  
5 a dummy cell. In a case where a dummy cell is inserted, the dummy insertion signal DUM (in which "0" indicates "normal" and "1" indicates "dummy insertion") is output.

The SAR-PDU header creation unit 71 creates the SAR-PDU header shown in Fig. 23 using CSI, SC contained  
10 in the SAR-PDU header that enters from the cell filter 50 as well as the cell-header valid/invalid determination signal INV and dummy insertion signal DUM that enter from the cell determination unit 51.

(1) When INV = "0", DUM = "0" hold, and when INV =  
15 "1", DUM = "0" hold, the selector 56 selects and outputs, 12 bytes at a time, the total of one byte of SAR-PDU data that has been created by the SAR-PDU header creation unit 71 and 47-byte cell-payload data from the second byte onward that has been stored in the cell  
20 accumulator 54 (see Fig. 23). (2) When INV = "1", DUM = "1" hold, the selector 56 selects and outputs, 12 bytes at a time, the total of one byte of SAR-PDU data that has been created by the SAR-PDU header creation unit 71 and 47-byte dummy data that has been generated  
25 by the dummy cell creation unit 55.

The pointer detector / P-format cell detector 72 is internally provided with a downcounter SPECTR that counts from 2357 to 0 to indicate 2358 byte positions

(see Fig. 12) of the AAL-1 cell conversion zone. The  
downcounter SPECTR is preset to the pointer value at the  
time of pointer detection, after which the downcounter  
counts down cyclically at the byte timing of the AAL-1  
5 cell conversion zone. Using the two high-order bits of  
the cell payload read out of the receive buffer 57 and  
the value of the count in the downcounter SPECTR, the  
pointer detector / P-format cell detector 72 executes  
pointer-detection / P-format determination processing,  
10 which is illustrated in Fig. 24, and outputs (1) the SDT  
pointer value (PTR value) and pointer-detection signal  
PTR-DET and (2) outputs a P-format cell determination  
signal PFORM.

In the flow of processing for pointer detection and  
15 P-format cell determination, the pointer detector / P-  
format cell detector 72 reads an SAR-PDU header (step  
101) and checks to see whether sequence count SC = 0  
holds (step 102). If SC = 0 holds ("YES" at step 101),  
a P-format cell detection signal ARDYPFMT is reset to  
20 "0" (step 103). The P-format cell detection signal  
ARDYPFMT is a signal that is reset to "0" at the  
beginning of one cycle of SC values 0 to 7; at detection  
of a P-format cell, the signal takes on the "1" level  
until it is reset.

25 Next, it is determined whether SC = 1, 3, 5 or 7  
holds (i.e., whether SC is odd) (step 104). If the SC  
is odd ("YES" at step 104), then the cell is a non-P-  
format cell. Accordingly, the operations VALIDPTR =

"0", NPORP = "0" are performed (step 105) and control returns to the beginning. VALIDPTR is a pointer detection signal that rises to logical "1" when a true SDT pointer has been detected, and NPORP is a signal  
5 that rises to logical "1" when a P-format cell has been detected.

If the SC is not odd ("NO" at step 104), it is determined whether the count in the downcounter SPECTR is a value in the range 0 to 93 at the starting octet  
10 position of the cell payload (step 106). If the value of the count falls within the range of 0 to 93 ("YES" at step 106), it is determined whether cell-header valid/invalid determination signal INV = "1" holds or whether dummy insertion signal DUM = "1" holds (step  
15 107). If either INV or DUM is "1" ("YES" at step 107), it is determined whether the P-format cell detection signal ARDYPFMT is "1" (step 108). If ARDYPFMT = "1" holds ("NO" at step 108), this means that a P-format cell has already been detected and therefore the  
20 operations VALIDPTR = "0", NPORP = "0" are performed (step 109). If ARDYPFMT = "0" holds ("YES" at step 108), this means that a P-format cell has not yet been detected and therefore it is assumed that a cell for which the SC value is even was the P-format cell. The  
25 operations VALIDPTR = "0", NPORP = "1", ARDYPFMT = "1" are performed (step 110) and control returns to the beginning.

If it is found at step 106 the count in the



downcounter SPECTR is not a value in the range 0 to 93  
("NO" at step 106) or if it is found at step 107 that  
INV = "0", DUM = "0" hold ("NO" at step 107), then it is  
determined whether the SC value is 6 (step 111). If the  
5 decision rendered is "YES", then it is determined  
whether cell-header valid/invalid determination signal  
INV = "1" holds or whether dummy insertion signal DUM =  
"1" holds (step 112). If either INV or DUM is "1"  
("YES" at step 112), it is determined whether the P-  
10 format cell detection signal ARDYPFMT is "1" (step 113).  
If ARDYPFMT = "1" holds ("NO" at step 113), this means  
that a P-format cell has already been detected. The  
operations VALIDPTR = "0", NPORP = "0", therefore, are  
performed (step 114). If ARDYPFMT = "0" holds ("YES" at  
15 step 113), this means that a P-format cell has not yet  
been detected and, hence, it is assumed that a cell for  
which SC value = 6 holds was the P-format cell. The  
operations VALIDPTR = "0", NPORP = "1", ARDYPFMT = "1"  
are performed (step 115) and control returns to the  
20 beginning.

If it is found at step 111 that SC value = 6 does  
not hold or if it is found at step 112 that INV = "0",  
DUM = "0" hold ("NO" at step 112), then it is determined  
whether the CSI = "1" holds (step 116). If CSI = "1"  
25 holds ("YES" at step 116), then it is determined whether  
INV = "0" holds (step 117). If INV = "0" holds ("YES"  
at step 117), then it is determined whether the value  
(pointer value) PTR of the second byte of the cell of

interest is a value in the range 0 to 93 (step 118). If the decision rendered is "YES", this means that the cell is a true P-format cell. The operations VALIDPTR = "1", NPORP = "1", ARDYPFMT = 1, therefore, are performed

5 (step 119) and control returns to the beginning.

However, if the pointer value PTR is not in the range 0 to 93 but is 127, the cell is a P-format cell but it is judged that the pointer is not a pointer indicating the frame reference position (i.e., that the pointer is a  
10 false pointer). The operations VALIDPTR = "0", NPORP = "1", ARDYPFMT = 1 are performed (step 120). If CSI = "0" or INV = "1" is found to hold at steps 116, 117, then it is judged that the cell is a non-P-format cell, the operations VALIDPTR = "0", NPORP = "0" are performed  
15 (step 121) and control returns to the beginning.

Thus, in accordance with the first embodiment, a cell (a dummy cell for which the SC value is even or an invalid cell for which the SC value is even) that has a high likelihood of being a P-format cell is assumed to  
20 be a P-format cell when a P-format cell has been lost. Furthermore, pointer timing is predicted using the value of the count recorded by the downcounter SPECTR. When a P-format cell has been lost at the predicted timing, a dummy cell or invalid cell for which the SC value is  
25 even at this timing is judged to be a P-format cell. As a result, judgment of P-format cells can be made with greater precision. By virtue of the foregoing, a correct P-format cell can be assumed in one cycle (SC =

0 ~ 7) and the IFL of a receive buffer can be prevented from fluctuating as a result of judging a P-format cell to be a non-P-format cell or judging a non-P-format cell to be a P-format cell.

5        Furthermore, even if a P-format cell is lost, the fact that a cell is assumed to be a P-format cell assures that a large quantity of reproduced data will not be lost as a consequence of loss of P-format cells.

10        (D)    Second embodiment of interface having band adjustment function

Fig. 25 is a diagram showing another construction of an interface provided on the exit side of an ATM network and having a band adjustment function. Components identical with those shown in Fig. 20 are  
15        designated by like reference characters. This arrangement differs in that (1) the SAR-PDU header creation unit 71 is provided; (2) the cell determination unit 51 outputs the cell-header valid/invalid determination signal INV and the dummy cell insertion  
20        signal DUM; (3) a data accumulator 73 for storing one cycle of cells (SC = 0 ~ 7) is provided in front of the receive buffer 57; and (4) a pointer correction controller 74 for correcting a pointer upon referring to the SAR-PDU header of each cell of one stored cycle of  
25        cells is provided in front of the receive buffer 57.

The cell valid/invalid judging unit 52, cell loss / erroneous insertion examining unit 53, cell accumulator 54, dummy cell creation unit 55, selector 56 and SAR-PDU

header creation unit 71 operate in the same manner as set forth in connection with the first embodiment of Fig. 20. Specifically, (1) when INV = "0", DUM = "0" hold, and when INV = "1", DUM = "0" hold, the selector 56 splits, 12 bytes at a time four times, the total of one byte of SAR-PDU data that has been created by the SAR-PDU header creation unit 71 and 47-byte cell-payload data from the second byte onward that has been stored in the cell accumulator 54, and outputs the result (see Fig. 23). (2) When INV = "1", DUM = "1" hold, the selector 56 splits, 12 bytes at a time four times, the total of one byte of SAR-PDU data that has been created by the SAR-PDU header creation unit 71 and 47-byte dummy data that has been created by the dummy cell creation unit 55, and outputs the result. The data accumulator 73 stores a payload of one cycle output from the selector 56, and the pointer correction controller 74 performs pointer correction, in accordance with the flowchart of pointer correction processing shown in Fig. 26, while referring to the SAR-PDU header of each cell of one cycle of accumulated cells.

Specifically the data accumulator 73 receives and accumulates a cell payload output from the selector 56 (step 201). The pointer correction controller 74 checks to see whether one cycle of cells has arrived (step 202). If one cycle of cells has accumulated, it is determined whether a cell for which CSI = "1" holds and for which the SC value is even exists (step 203). If

5

15

25

(step 211). If there are two cells for which CSI = "1" holds and for which the SC values are even, it is decided that the cell for which INV = "0", DUM = "0" hold and for which the SC value is even is a P-format cell (step 212) and the CSI of the cell for which INV = "1" or DUM = "1" holds and for which SC value is even is corrected to "0" (step 213).

A cell that has been corrected by the above-described processing is stored in the receive buffer 57, after which control similar to that of the embodiment shown in Fig. 20 is carried out and user data is sent from the receive buffer 57 to the STS-3 frame assembler 62.

Thus, in accordance with the second embodiment, a cell (a dummy cell for which the SC value is even or an invalid cell for which the SC value is even) that has a high likelihood of being a P-format cell is assumed to be a P-format cell when a P-format cell has been lost. As a result, P-format cells can be assumed correctly every cycle (SC = 0 ~ 7) and the IFL of a receive buffer can be prevented from fluctuating as a result of judging a P-format cell to be a non-P-format cell or judging a non-P-format cell to be a P-format cell.

Further, in accordance with the second embodiment, even if a P-format cell is lost, the fact that a cell is assumed to be a P-format cell correctly assures that a large quantity of reproduced data will not be lost as a consequence of loss of P-format cells.

(E) Third embodiment of interface having band adjustment function

Fig. 27 is a diagram showing another construction of an interface provided on the exit side of an ATM network and having a band adjustment function. Components identical with those shown in Fig. 25 are designated by like reference characters. This arrangement differs in that (1) a data accumulator 75 for one cell is provided in front of the receive buffer 57, and (2) a pointer correction controller 76 for correcting a pointer in accordance with the flowchart of Fig. 28 upon referring successively to the SAR-PDU headers of cells is provided in front of the receive buffer 57.

In the flowchart of Fig. 28 illustrating processing for pointer correction, the pointer correction controller 76 determines whether CSI = "1" holds for every cell for which SC is an even number (step 301). If CSI = "1" holds, it is decided that the cell for which the SC value is even is a P-format cell (step 302).

If a cell for which CSI = "1" holds does not exist among cells for which SC = 0, SC = 2, SC = 4, SC = 6 hold, however, the cell for which SC = 6 holds is decided upon as being the P-format cell (step 303), the CSI of the SAR-PDU header (first byte) in the payload for which SC = 6 holds is made "1" and the pointer value (second byte) is made 127 (indicative of a false

pointer) (step 304).

Thus, in accordance with the third embodiment, it is determined, cycle by cycle, whether a cell for which the SC value is even is a P-format cell. When a P-format cell has been lost, it is assumed that the cell for which SC = 6 holds is a P-format cell. As a result, the data accumulator for one cycle employed in the second embodiment may be dispensed with, thereby making it possible to assume that a cell is a P-format cell through a simpler arrangement.

Specifically, in accordance with the third embodiment, in a case where a cell that has been lost exists on the side of an ATM network, processing can be simplified over that of the second embodiment by taking into consideration the fact that the content of STS-3 frame data cannot be reproduced normally in such case. Moreover, coincidence of the bands corresponding to both the STS-3 and ATM networks can be assured.

(E) Fourth embodiment of interface having band adjustment function

Fig. 29 is a diagram showing the construction of a fourth embodiment of an interface provided on the exit side of an ATM network and having a band adjustment function. Components identical with those shown in Fig. 25 are designated by like reference characters. This arrangement differs in that the data accumulator 73 for one cycle and pointer correction controller 74 are provided on the output side (read-out side) of the



receive buffer 57. This is the difference between whether pointer correction control is performed before a cell payload is written to the receive buffer (the second embodiment) and whether pointer correction control is performed after a cell payload is read out of the receive buffer (the third embodiment). The way in which pointer correction control is performed, however is the same.

It should be noted that the data accumulator 75 and pointer correction controller 76 in the third embodiment can similarly be provided on the read-out side of the receive buffer 57.

The fourth embodiment provides effects similar to those of the third embodiment.

Thus, in accordance with the present invention, the necessary part of overhead and payload are adopted as a cell conversion zone, whereby transmission band can be reduced. Moreover, since a pointer specifying the reference position (e.g., starting position) of the cell conversion zone is included in a cell, the original frame format can be assembled from received cells.

Further, in accordance with the present invention, if a P-format cell is lost owing to cell loss or cell garbling, etc., a P-format cell can be generated, it can be so arranged that the IFL set for a receive buffer will not fluctuate, and it can be so arranged that starvation and overflow will not occur.

Further, in accordance with the present invention,

a cell (a dummy cell for which the SC value is even or an invalid cell for which the SC value is even) that has a high likelihood of being a P-format cell is assumed to be a P-format cell when a P-format cell has been lost.

5 As a result, a cell can be assumed to be a P-format cell correctly every cycle ( $SC = 0 \sim 7$ ) and the IFL of a receive buffer can be prevented from fluctuating as a result of judging a P-format cell to be a non-P-format cell or judging a non-P-format cell to be a P-format  
10 cell. Moreover, even if a P-format cell is lost, the fact that a prescribed cell is assumed to be a P-format cell assures that a large quantity of reproduced data will not be lost as a consequence of loss of P-format cells.

15 Further, in accordance with the present invention, pointer timing is predicted using the value of a count recorded by a downcounter SPECTR. When a P-format cell is lost at the predicted timing, a prescribed cell is judged to be a P-format cell based upon this timing.  
20 This makes it possible to raise the precision with which P-format cells are judged. As a result, it is possible to make an assumption of a correct P-format cell in one cycle ( $SC = 0 \sim 7$ ), and the IFL of a receive buffer can be prevented from fluctuating as a result of judging a  
25 P-format cell to be a non-P-format cell or judging a non-P-format cell to be a P-format cell. Furthermore, even if a P-format cell is lost, the fact that a prescribed cell is assumed to be a P-format cell assures

that a large quantity of reproduced data will not be lost as a consequence of loss of P-format cells.

Further, in accordance with the present invention, when a P-format cell is lost at a predicted timing, a  
5 dummy cell for which the SC value is even or an invalid cell for which the SC value is even at this timing is judged to be a P-format cell. This makes it possible to raise the precision with which P-format cells are judged.

10 Further, in accordance with the present invention, whether a cell having an even-numbered SC value is a P-format cell is checked successively every cycle and, when a P-format cell is lost, a cell for which SC is equal to 6 is assumed to be a P-format cell. As a  
15 result, P-format cells can be inferred through a simple arrangement without requiring the provision of a data accumulator for one cycle. and it possible to assure agreement between the bands of STS-3 and ATM networks.

As many apparently widely different embodiments of  
20 the present invention can be made without departing from the spirit and scope thereof, it is to be understood that the invention is not limited to the specific embodiments thereof except as defined in the appended claims.